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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,896	04/30/2001	Steven Towle	884.409US1	4065

7590 03/31/2004

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EXAMINER
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PAREKH, NITIN

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/845,896

Applicant(s)

TOWLE ET AL.

Examiner

Nitin Parekh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 08 December 2003.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-18 and 24-35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 and 24-35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04-30-01 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 6-10, 18, 24 and 27 are rejected under 35 U.S.C. 102(a) as being anticipated by Brooks et al. (US Pat. 6084297).

Regarding claim 1, Brooks et al. disclose a microelectronic device package/electrical system (10 in Fig. 2) comprising:

- a die (14 in Fig. 1 and 2) fixed within a package core (40/8 in Fig. 2), the package core being made of an adhesively coated frame/board-shaped dielectric material/insulating film having first insulating solder mask surface (8 in Fig. 2, Col. 6, line 1-34),
- the package core having a metallic layer/cladding of copper (50 in Fig. 2) at the top surface providing a ground/reference plane and improved rigidity and thermal dissipation (Col. 6, lines 35-45)

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- a metallization layer built upon the die and the package core (36/22 in Fig. 2) the metallization layer having a first metallization portion located over the die (36 in Fig. 2) and a second metallization portion (22 in Fig. 2) located over the package core
- a grid array interposer unit/laminated substrate (16 in Fig. 2) laminated to the metallization layer, the interposer having an array of electrical contacts/solder balls (26 in Fig. 2) on a second surface, and
- a carrier substrate/board (30 in Fig. 2) having a second array of electrical contacts/circuitry (28 in Fig. 2), the respective contacts of the interposer and the carrier substrate/board being conductively coupled through the solder balls (Fig. 1 and 2; Col. 5, line 15- Col. 7, line 25).

Regarding claim 2, Brooks et al. disclose substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. disclose the metallization layer including the first metallization portion located over the die (36 in Fig. 2) and the second metallization portion (22 in Fig. 2) located over the package.

Regarding claim 6, Brooks et al. disclose substantially the entire claimed structure as applied to claim 1 above, and further disclose the die being fixed within the package core using an encapsulation material (54 in Fig. 2- Col. 7, line 20).

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Regarding claim 7, Brooks et al. disclose substantially the entire claimed structure as applied to claim 1 above, wherein Brooks et al. disclose the package core having the metallic layer/cladding of copper (50 in Fig. 2) at the top surface (Col. 6, lines 35-45).

Regarding claims 8-10, Brooks et al. disclose substantially the entire claimed structure as applied to claims 1 and 7 above, and Brooks et al. further disclose the metallic layer/cladding being coupled to ground, reference or power during operation of the device to provide the respective ground, reference or power plane/source for the wiring/transmission structure (Col. 6, lines 24-30; Col. 6, lines 45-48; Col. 7, lines 1-5) within the metallization layer through conductive vias, traces and conductive sites/pads (52/34, 32 and 44/24 respectively in Fig. 1 and 2) including the ground pad, the ground, reference or power connections being selected based on the application requirements (Col. 7, line 4).

Regarding claim 18, Brooks et al. disclose substantially the entire claimed structure as applied to the claim 1 above, wherein the metallization between the die and the grid array interposer being a single metallization layer (36 in Fig. 2).

Regarding claim 24, Brooks et al. disclose substantially the entire claimed structure as applied to the claim 1 above, wherein the electrical system comprises the die/core assembly having the substrate/circuit board (14/40 and 30 respectively in Fig. 1 and 2).

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Regarding claim 27, Brooks et al. disclose substantially the entire claimed structure as applied to the claim 24 above, wherein the first array of electrical contacts include the plurality of solder balls (26 in Fig. 2).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Kelly et al. (US Pat. 5798567).

Regarding claim 3, Brooks et al. teach substantially the entire claimed structure as applied to the claim 1 above, except connecting at least one decoupling capacitor to the second surface of the grid array interposer unit to provide decoupling for the circuitry within the die.

Kelly et al. teach using decoupling capacitors (67 in Fig. 5) connected to the second surface of the grid array interposer/substrate to improve the electromagnetic interference (EMI) suppression and the electrical performance of the integrated circuit package (Col. 4, line 25-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one decoupling capacitor being connected to the second surface of the grid array interposer unit as taught by Kelly et al so that the EMI can be reduced and the desired decoupling for the circuitry can be achieved in Brooks et al's device.

5. Claims 4, 32 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Sylvester (US Pat. 6014317).

Regarding claims 4 and 32, Brooks et al. teach substantially the entire claimed structure as applied to the claim 1 above, except the interposer having a thickness between the first and second surfaces being no greater than 0.5 mm.

Sylvester teaches using a grid array interposer unit/multilayered substrate (MLS 12 in Fig. 2) having the substrate thickness between the first and second surface such as about 2 mils, 3.9 mils, etc. (Col. 3, lines 10-15; Col. 24, line 5) to provide the desired stress reduction and surface irregularities (Col. 3, line 12), the thickness being no greater than 0.5 mm.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate except the interposer having a thickness between the first and second surfaces being no greater than 0.5 mm as taught by Sylvester so that the surface irregularities and the compressive stress can be reduced in Brooks et

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al's device.

Regarding claim 35, Brooks et al. and Sylvester teach substantially the entire claimed structure as applied to claim 32 above, and Brooks et al. further teach the metallic layer/cladding being coupled to ground, reference or power during operation of the device to provide the respective ground, reference or power plane/source for the wiring/transmission structure (Col. 6, lines 24-30; Col. 6, lines 45-48, Col. 7, lines 1-5) within the metallization layer through conductive vias, traces and conductive sites/pads including the ground pad (52/34, 32 and 44/24 respectively in Fig. 1 and 2), the ground, reference or power connections being selected based on the application requirements (Col. 7, line 4).

6. Claims 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Harada et al. (US Pat. 5523622).

Regarding claims 11 and 12, Brooks et al. teach substantially the entire claimed structure as applied to claim 1 above, and further disclose an embodiment having the die being flip-chip bonded (Fig. 5; Col. 8, lines 3-30), but fail to teach the die including a plurality of power bars and ground bars distributed on the surface where each of the power and ground bars being conductively coupled to respective multiple power and ground pads of the die, power bars and ground bars being interleaved within a central



region the surface of the die.

Harada et al. teach using a metallization pattern on a die where a plurality of power bars and ground bars are distributed on the surface and interleaved within a central region of the die where each of the power and ground bars (not numerically referenced in Fig. 1- see power and ground bar pattern in the central region) being conductively coupled to respective multiple power and ground pads (218d and 218e in Fig. 1 and 5) of the die (Col. 5, line 57- Col. 6, line 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of power bars and ground bars distributed on the surface where each of the power and ground bars being conductively coupled to respective multiple power and ground pads of the die as taught by Harada et al so that the ground potential can be stabilized and the transmission characteristics can be improved in Brooks et al's device.

Regarding claim 13, Brooks et al. disclose substantially the entire claimed structure as applied to claims 1 and 11 above, except the die including a plurality of signal contact pads being distributed within a peripheral region of the surface of the die.

Harada et al. teach using a metallization pattern on the die where a plurality of signal contact pads (218a, and 218b in Fig. 5) is distributed within central and peripheral regions of the surface of the die (Fig. 1 and 5., Col. 5, line 57- Col. 6, line 40).

It would have been obvious to a person of ordinary skill in the art at the time

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invention was made to incorporate a plurality of signal contact pads being distributed within a peripheral region of the surface of the die as taught by Harada et al. so that the transmission characteristics can be improved in Brooks et al's device.

Regarding claims 14 and 15, Brooks et al. disclose substantially the entire claimed structure as applied to claim 1 above, but fails to specify the metallization layer including at least power or ground landing pad being situated over the die being conductively coupled to multiple power or ground bond pads respectively through corresponding via connections.

Harada et al. teach using a metallization pattern on the die and the substrate where a power or a ground landing pad (not numerically referenced - see the power or ground landing pad situated above the via connecting the power layer 208 or ground layer 207 in Fig. 2) is conductively coupled to multiple power bond pads (218d in Fig. 5) through corresponding via connections (see vias 216 in Fig. 2, Col. 5, lines 1- Col. 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least power landing pad being conductively coupled to multiple power bond pads through corresponding via connections as taught by Harada et al so that the power, signal and ground routing can be improved and the transmission loss can be reduced in Brooks et al's device.

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Regarding claims 16 and 17, Brooks et al. and Harada et al. teach substantially the entire claimed structure as applied to claims 1, 11, 13 and 14 above, and Brooks et al. further teach the metallization layer including at least one ground or power conductive site/landing pad (44 in Fig. 1 and 2) being situated over the package core and being conductively coupled to the respective multiple power or ground conductive site/bond pad on the die through the respective trace portion (32 in Fig. 1 and 2) extending over the die and a plurality of via (34 in Fig. 1 and 2) connections (Col. 6, line 25- Col. 7, line 10).

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Taniguchi et al. (US Pat. 6388333).

Regarding claim 25, Brooks et al. teach substantially the entire claimed structure as applied to claim 24 above, except the circuit board being a computer motherboard.

Taniguchi et al. teach using a semiconductor mounting device/system having a variety of configurations including conventional substrates such as motherboard/computer motherboard (38 in Fig. 28, Col. 17, lines 30-35, Col. 11, lines 10-20).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a computer motherboard as the substrate as taught

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by Taniguchi et al. so that the desired mounting and external connection requirements can be achieved in Brooks et al's device.

8. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) in view of Blish, II et al (US Pat. 6049465).

Regarding claim 26, Brooks et al. teach substantially the entire claimed structure as applied to claim 24 above, except the first array of contacts including a plurality of pins.

Blish, II et al. teach using electrical contacts such as pins (150 in Fig. 1), balls, etc. to provide an external connection between the carrier/interposer and a PWB (Col. 1, line 30-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first array of contacts including a plurality of pins as taught by Blish, II et al. so that the integrity and reliability of the external connection can be improved in Brooks et al's device.

9. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) and Sylvester (US Pat. 6014317) as applied to claim 32 and further in view of Kelly et al (US Pat. 5798567).

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Regarding claim 33, Brooks et al. and Sylvester teach substantially the entire claimed structure as applied to the claim 32 above, except connecting at least one decoupling capacitor to the second surface of the grid array interposer unit to provide decoupling for the circuitry within the die.

Kelly et al. teach using decoupling capacitors (67 in Fig. 5) connected to the second surface of the substrate to improve the electromagnetic interference (EMI) suppression and the electrical performance of the integrated circuit package (Col. 4, lines 25-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to connect at least one decoupling capacitor to the second surface of the grid array interposer unit to provide decoupling for the circuitry within the die as taught by Kelly et al. so that the EMI and thickness of the package can be reduced and the desired decoupling for the circuitry can be achieved in Sylvester and Brooks et al's device.

10. Claims 5 and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) and Degani et al. (US Pat. 5608262) as applied to claims 1 and 24 above, and further in view of Kelly et al. (US Pat. 5798567) and Harada et al. (US Pat. 5523622).

Regarding claims 5, 28 and 31, Brooks et al. teach substantially the entire claimed structure as applied to the claims 1 and 24 respectively above, wherein the electrical system further comprises the die/core assembly (14/40 in Fig. 1 and 2), but Brooks et al. fail to teach the interposer unit including an opening that exposes a first portion of the metallization layer and at least one decoupling capacitor being connected to the first portion/exposed portion of the metallization layer to provide decoupling for the circuitry within the die.

Degani et al. teach using a composite printed wiring board (PWB) substrate (36 in Fig. 10) having an upper level PWB and a lower level/interposer PWB (38 and 37 respectively in Fig. 10). The lower level/interposer PWB further includes an opening that exposes a portion of the metallization layer under the silicon substrate having components such as chips being connected thereon to reduce thickness of a package (16 and 17 in Fig. 10., Col. 6, lines 40-65).

Kelly et al. teach using decoupling capacitors (67 in Fig. 5) connected to the second surface of the substrate to improve the electromagnetic interference (EMI) suppression and the electrical performance of the integrated circuit package (Col. 4, line 25-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the interposer unit including an opening that exposes a first portion of the metallization layer and at least one decoupling capacitor being connected to the first portion of the metallization layer as taught by Degani et al. and

Kelly et al. so that the EMI and thickness of the package can be reduced and the desired decoupling for the circuitry can be achieved in Brooks et al's device.

Regarding claims 29 and 30, Brooks et al., Degani et al. and Kelly et al. teach substantially the entire claimed structure as applied to the claim 28 above, except the metallization layer including at least one power or ground landing pad being situated over the die or the package core and further being conductively coupled to multiple power or ground bond pads respectively through corresponding via connections.

Harada et al. teach using a metallization pattern on the die and the substrate where a power or a ground landing pad (not numerically referenced - see the power or ground landing pad situated above the via connecting the power layer 208 or ground layer 207 in Fig. 2) is conductively coupled to multiple power bond pads (218d in Fig. 5) through corresponding via connections (see vias 216 in Fig. 2., Col. 5, lines 1- Col. 40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one power landing pad located over the die or the package core being conductively coupled to multiple power bond pads through corresponding via connections as taught by Harada et al so that the power, signal and ground routing can be improved and the transmission loss can be reduced in Degani et al., Kelly et al Brooks et al's device.

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11. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brooks et al. (US Pat. 6084297) and Sylvester (US Pat. 6014317) as applied to claim 32 above, and further in view of Degani et al. (US Pat. 5608262) and Kelly et al (US Pat. 5798567).

Regarding claim 34, Brooks et al. and Sylvester teach substantially the entire claimed structure as applied to the claim 32 above, except the interposer unit including an opening that exposes a first portion of the metallization layer and at least one decoupling capacitor being connected to the first portion of the metallization layer to provide decoupling for the circuitry within the die.

Degani et al. teach using a composite printed wiring board (PWB) substrate (36 in Fig. 10) having an upper level PWB and a lower level/interposer PWB (38 and 37 respectively in Fig. 10). The lower level/interposer PWB further includes an opening that exposes a portion of the metallization layer under the silicon substrate having components such as chips being connected thereon to reduce thickness of a package (16 and 17 in Fig. 10', Col. 6, lines 40-5).

Kelly et al. teach using decoupling capacitors (67 in Fig. 5) connected to the second surface of the substrate to improve the electromagnetic interference (EMI) suppression and the electrical performance of the integrated circuit package (Col. 4, line 25-40).

It would have been obvious to a person of ordinary skill in the art at the time



invention was made to incorporate the interposer unit including an opening that exposes a first portion of the metallization layer and at least one decoupling capacitor being connected to the first portion of the metallization layer as taught by Degani et al. and Kelly et al. so that the EMI and thickness of the package can be reduced and the desired decoupling for the circuitry can be achieved in Sylvester and Brooks et al's device.

### ***Response to Arguments***

12. Applicant's arguments filed on 12-08-03 have been fully considered but they are not persuasive.

A. Applicant contends that Brooks et al. do not teach a metallization layer built up upon the die and the package core.

However, Fig. 2 in Brooks et al. clearly shows a metallization layer built upon/disposed on the die and the package core (36 and 22 respectively in Fig. 2), the metallization layer having the first portion being located over the die (see 36 in Fig. 2) and the second metallization portion (see 22 in Fig. 2) located over the package core (Col. 5, lines 45-54).

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B. Applicant contends that in Brooks et al's structure as shown in Fig. 2, the die and the adhesive do not form a continuous surface upon which the metallization layer can be built.

However, such limitations have not been recited in any of the independent claims and the dependent claims thereof.

### ***Conclusion***

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP  
03-21-04



EDDIE LEE  
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